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EXAMINER	
WHIPKEY, JASON T	

ART UNIT	PAPER NUMBER
2622	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/827,333	SU ET AL.	
	Examiner	Art Unit	
	Jason T. Whipkey	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because it begins with the phrase, "The present invention describes". Correction is required. See MPEP § 608.01(b).

Claim Objections

2. The claims appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors.

3. Claims 1, 3, 4, 6, 7, and 9 are objected to because of the following informalities:

- In claim 1 on line 3, it appears that "photos" should read, -- photons --.
- In claim 3 on line 2, it appears that "operation amplifier" should read, -- operational amplifier --.
- In claim 4 on line 1, it appears that "operation amplifier" should read, -- operational amplifier --.
- In claim 4 on lines 3-4, "certain circuit inside" is unclear.
- In claim 4 on line 5, it appears that "area" should read, -- are a --.
- In claim 6 on line 2, "that be" is unclear.
- In claim 7 on lines 1-2, it appears that "a sample and a hold circuit" should read, -- a sample and hold circuit --.

- In claim 7 on line 2, it appears that "operation amplifiers" should read, -- operational amplifiers --.
- In claim 9 on lines 3 and 5, "while switch turning" is unclear.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 9 and 10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Regarding **claim 9**, line 5 recites "a bright voltage". This term appears once in the specification and is not defined.

Claim 10 recites that the switch "includes a NMOS transistor ... the switch **is** a PMOS transistor ... and the switch **is** a CMOS transistor" (emphasis added). The specification does not explain how a single switch is all of these. For examination purposes, the claim will be treated as if it recites one of these types.

Claim 10 recites "a CMOS transistor". There is no accepted definition for this term, as a CMOS device comprises a number of transistors.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Claim 2 recites "a photodiode adapted for both N-sub and P-sub of CMOS process". This is unclear.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1, 9 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Bock (U.S. Patent Application Publication No. 2002/0033439).

Regarding **claim 1**, Bock discloses an integrated image detecting apparatus (see Figure 3) used in CMOS process (see paragraph 17), comprising:

an optical detecting element (photodiode 60) is operated to detect an optical variation and convert photons into charge (see paragraph 20);

an integrated circuit (the device is formed as a monolithic integrated circuit; see paragraph 17) is operated to convert charge produced by the optical detecting element into electronic signal that is a different type voltage (inherently performed by source-follower transistor M2; see paragraph 21);

a correlated double sampling circuit connects to read the electronic signal of the integrated circuit output for canceling variation of the optical detecting element and of the integrated circuit (see paragraph 22); and

an output circuit (readout circuit 52) performs the output signal of the correlated double sampling circuit and output a plurality of signals (70 and 72; see paragraph 22).

Regarding **claim 9**, Bock discloses the different type voltage of the output signal for the integrated circuit further comprising:

a reset voltage (RST) operated while switch turning on inside the integrated circuit (see paragraph 20); and

a bright voltage (ROW) operated while switch turning off inside the integrated circuit (as shown in Figure 5, ROW is high when RST is low).

Regarding **claim 10**, Bock discloses:

the switch includes a NMOS transistor turned on at high voltage and turned off at low voltage (see paragraph 20), or the switch is a PMOS transistor turned on at low voltage and turned off at high voltage, or the switch is a CMOS transistor turned on and turned off at both said high-low voltage.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

12. Claims 1, 7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuno (U.S. Patent Application Publication No. 2002/0190193) in view of Ikeda (U.S. Patent No. 6,111,606).

Regarding **claim 1**, Mizuno discloses an integrated image detecting apparatus (see Figure 6) used in CMOS process, comprising:

an optical detecting element (photodiode PD) is operated to detect an optical variation and convert photons into charge (see paragraph 39);

an integrated circuit (operational amplifier A_1 is inherently an IC; see paragraph 41) is operated to convert charge produced by the optical detecting element into electronic signal that is a different type voltage (see paragraphs 43 and 97);

a correlated double sampling circuit (20) connects to read the electronic signal of the integrated circuit output for canceling variation of the optical detecting element and of the integrated circuit (see paragraphs 84-87); and

an output circuit (sample and hold circuit 30) performs the output signal of the correlated double sampling circuit (see paragraph 88).

Mizuno is silent with regard to outputting a plurality of signals.

Ikeda discloses a signal processor for an imaging device (see Figure 9), wherein sample-and-hold circuit components 69 and 70 each output a signal.

An advantage of outputting two signals is that a slower sample-and-hold circuit can be used, thereby reducing the need for more expensive high-speed components. For this reason, it

would have been obvious to one of ordinary skill in the art at the time the invention was made to have Mizuno's system output a plurality of signals.

Regarding **claim 7**, Ikeda discloses:

> the output circuit comprises a sample and a hold circuit (69 and 70; see column 11, lines 11-15) and a plurality of unit gain operation amplifiers (operational amplifiers 75 and 76 are used as buffers, which inherently have a gain of unity; see column 12, lines 30-31).

Regarding **claim 8**, Ikeda discloses:

> the unit gain operation amplifier is a single stage amplifier (see Figure 9).

Ikeda is silent with regard to the type of transistors that comprise the operational amplifier.

Official Notice is taken that it was well known in the art at the time the invention was made to use NMOS and/or PMOS transistors in an operational amplifier. An advantage of doing so is that the resulting operational amplifier requires less power and produces lower noise. For this reason, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Mizuno's system use NMOS or PMOS transistors in an operational amplifier.

13. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuno in view of Ikeda and further in view of Wang (U.S. Patent No. 6,518,085).

Claim 2 can be treated like claim 1. However, Mizuno is silent with regard to the construction details of the photodiode.

Wang discloses a CMOS imager, wherein:

the optical detecting element is a photodiode adapted for both N-sub and P-sub of CMOS process (see column 4, lines 33-39).

As described in column 4, lines 33-39, an advantage of using such a photodiode is that it has a uniform spectral response. For this reason, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Wang's system include a photodiode adapted for "both an N-sub and P-sub of CMOS process".

14. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuno in view of Ikeda and further in view of Iida (U.S. Patent Application Publication No. 2003/0057372) and Sakamoto (U.S. Patent No. 4,672,453).

Claim 3 can be treated like claim 1. Additionally, Mizuno discloses:

the integrated circuit comprises an operational amplifier (A_1; see Figure 6), a reference voltage (V_{inp1}), an electric charge storing device (capacitor Cf_1), and a switch (SW_{11}).

Mizuno is silent with regard to including a CMOS inverter.

Iida discloses an imaging device that includes the amplifier shown in Figure 8. CMOS inverters 36A and 36B — shown in detail in Figure 9 — are included after operational amplifier 30 (see paragraph 99).

As stated in paragraph 100, an advantage of including a CMOS inverter is that noise can be reduced. For this reason, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Mizuno's system include a CMOS inverter.

Mizuno is also silent with regard to the switch being a CMOS switch.

Sakamoto discloses an image sensor with a CMOS switch connected to an amplifier. As stated in column 9, lines 59-61, an advantage of using a CMOS switch is that noise can be cancelled. For this reason, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Mizuno's system include a CMOS switch.

Regarding **claim 4**, Mizuno's device includes:

> the operational amplifier is a single stage amplifier (see Figure 6), and the reference voltage is an external voltage source or a bias provided by certain circuit inside (voltage V_{inp1} inherently has a voltage source, which logically must be located either internally or externally), and the electric charge storing device is a capacitor (Cf_1).

Mizuno is silent with regard to the type of transistors that comprise the operational amplifier.

Official Notice is taken that it was well known in the art at the time the invention was made to use NMOS and/or PMOS transistors in an operational amplifier. An advantage of doing so is that the resulting operational amplifier requires less power and produces lower noise. For this reason, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Mizuno's system use NMOS or PMOS transistors in an operational amplifier.

As described *supra*, Iida shows that the CMOS inverter includes NMOS and PMOS transistors.

As described *supra*, Sakamoto discloses a CMOS switch. CMOS switches inherently include NMOS and PMOS transistors.

15. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuno in view of Ikeda and further in view of Sakamoto.

Claim 5 can be treated like claim 1. Additionally, Mizuno discloses (see Figure 6):

> the correlated double sampling circuit comprised an ac couple device (capacitor C_{22}), a switch (SW_2), and a unit gain operational amplifier (buffer A_2; see paragraphs 85-87).

Mizuno is also silent with regard to the switch being a CMOS switch. Sakamoto discloses an image sensor with a CMOS switch connected to an amplifier. As stated in column 9, lines 59-61, an advantage of using a CMOS switch is that noise can be cancelled.

For this reason, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Mizuno's system include a CMOS switch.

Regarding **claim 6**, Mizuno discloses:

> the ac couple device is a capacitor (C_{22}), and the unit gain operation amplifier is a single stage amplifier (see Figure 6).

Mizuno is silent with regard to the type of transistors that comprise the operational amplifier.

Official Notice is taken that it was well known in the art at the time the invention was made to use NMOS and/or PMOS transistors in an operational amplifier. An advantage of doing so is that the resulting operational amplifier requires less power and produces lower noise. For this reason, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Mizuno's system use NMOS or PMOS transistors in an operational amplifier.

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Whipkey, whose telephone number is (571) 272-7321. The examiner can normally be reached Monday through Friday from 9:00 A.M. to 5:30 P.M. eastern daylight time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivek Srivastava, can be reached at (571) 272-7304. The fax phone number for the organization where this application is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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June 12, 2007

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